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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/273,784	03/22/1999	JOHN G. MCBRIDE	10971308-1	7570

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EXAMINER	
PHAN, THAI Q	
ART UNIT	**PAPER NUMBER**
2123	17

DATE MAILED: 10/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PP9

Office Action Summary	Application No. 09/273,784	Applicant(s) John McBride
	Examiner Thai Phan	Art Unit 2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Jul 15, 2003* .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1, 2, 8, 9, 15, and 16* is/are rejected.

7) ☒ Claim(s) *3-7, 10-14, and 17-20* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This Office Action is in response to applicant's response filed on July 15, 2003. Claims 1-20 are pending in this Office Action.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 8, 9, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Provisional Application no. 60/093,830, filed on July 22, 1998, or US patent no. 6,499,129 B1 issued to Srinivasan et al.

As per claims 1 and 15, in the provisional application, Srinivasan discloses method and system for estimating design performances, including handling cross-coupling effects, simultaneous switching, etc. for device characterization including noise analysis or noise immunity with feature limitations similar to the claimed invention (Summary of the Invention, page 5, lines 18-26, for example). According to Srinivasan, the method and system for design rule checking includes a computer configured to execute a rule checker program (page 5, lines 18-26), wherein the design rule being checked for an integrated circuit design having gates, gate connected in datapath or along circuit paths including static gate characteristics, transistor

parameters such as transistor widths, lengths, connected in device channel, etc. ("Summary of the Invention", pages 5 and 6, for instance). The design rule checker program is to check transistor performance such as timing, cross-talk due to wire coupling, switching delay (pages 5, 6, 7, 8, for example). Srinivasan does not especially disclose checking noise immunity.

Practitioner in the art at the time of the invention was made would have found Srinivasan disclosure of checking circuit performance above would imply the claimed step for checking noise immunity because Srinivasan rule checker program is for verification of tight coupling wires in gate channel connected components (pages 5-8), for example, and it would be known in the art such tightly coupling channel connected components would contribute to noise, switching delay in order to verify noise immunity.

As per claim 2, Srinivasan discloses reading transistor design parameters such as channel length, gate width, length, and the likes for design rule check as claimed. Such transistor circuit design in static gate under rule checking would include for example inverter gate, p-channel and n-channel transistor, CMOS channel parameters, design parameters, etc. as well-known in transistor circuit design, and the rule checking of the gate circuit statically verifies device characteristics and performance analysis such as noise susceptibility or noise immunity in a specified design operation bound within thresholds values as known in MOS and CMOS of the circuit design (page 3, lines 9-16, page 5, lines 18-26, pages 6-9).

As per claim 8, Srinivasan discloses method and system for estimating design performances, including handling cross-coupling effects, simultaneous switching, etc. for device characterization including noise analysis or noise immunity with feature limitations similar to the

the claims (Summary of the Invention, page 5, lines 18-26, for example). According to Srinivasan, the method and system for design rule checking includes a computer configured to execute a rule checker program (page 5, lines 9-26), wherein the design rule being checked for an integrated circuit design having gates, gate connected in datapath or along circuit paths including static gate characteristics, transistor parameters such as transistor widths, lengths, connected in device channel, etc. ("Summary of the Invention", pages 5 and 6, for instance). The design rule checker program is to check transistor performance such as timing, cross-talk due to wire coupling, switching delay (pages 5, 6, 7, 8, for example). Srinivasan does not especially disclose checking noise immunity.

Practitioner in the art at the time of the invention was made would have found Srinivasan disclosure of checking circuit performance above would imply the claimed step for checking noise immunity because Srinivasan rule checker program is for verification of tight coupling wires in gate channel connected components (pages 5-8), for example, and it would be known in the art such tightly coupling channel connected components would contribute to noise, switching delay, etc. In other words, the noise analysis is for verification of noise immunity.

As per claim 9, Srinivasan discloses reading transistor design parameters for design rule check as claimed. Such transistor circuit design in static gate under rule checking would include for example inverter gate, p-channel and n-channel transistor, CMOS channel parameters, design parameters, etc. as well-known in transistor circuit design, and the rule checking of the gate circuit statically verifies device characteristics and performances such as cross-coupling which

would contribute to noise or noise susceptibility in a region of operation bound by threshold values as known in MOS device operation (Background of the Invention, pages 5-8).

As per claim 16, Srinivasan discloses reading transistor design parameters for design rule check as claimed. Such transistor circuit design in static gate under rule checking would include for example inverter gate, p-channel and n-channel transistor, CMOS channel parameters, design parameters, etc. as well-known in transistor circuit design, and the rule checking of the gate circuit statically verifies device characteristics or noise susceptible for device characterization and performance analysis (pages 5-8).

Allowable Subject Matter

3. Claims 3-7, 10-14, and 17-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Dependent claims 3-7, 10-14, and 17-20 are objected to because the claims require a plurality of checking models for rule checking program and method, each rule checking model is associated with ratio of the width of the P-field transistor to the width of the N-field transistor, the ratio corresponding to the numerical value stored in the memory device. In each checking model, the rule checker program obtaining a (first) ratio of the width of the n and p-type transistor of the first model, the first ratio used to access the first and second threshold values stored in the memory device, the rule checker program determines noise levels on the inputs taking possible high or low values, and compares the determined noise levels to the first and

second threshold values to determine the gate meets acceptable noise immunity requirement with respect to each model as claimed herein. The closest prior art of record does not expressly disclose such limitations as in the dependent claims.

Response to Arguments

4. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 6,591,402 B1, issued to Chandra et al., on July 2003

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thai Phan whose telephone number is (703) 305-3812.

7. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703)305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306, (for formal communications intended for entry)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

October 1, 2003

Thaiphan
Patent Examiner
AU 2123
Thai Phan